



# LC7533

## 3V Electronic Volume Control

### Use

- Attenuation of signal.

### Features

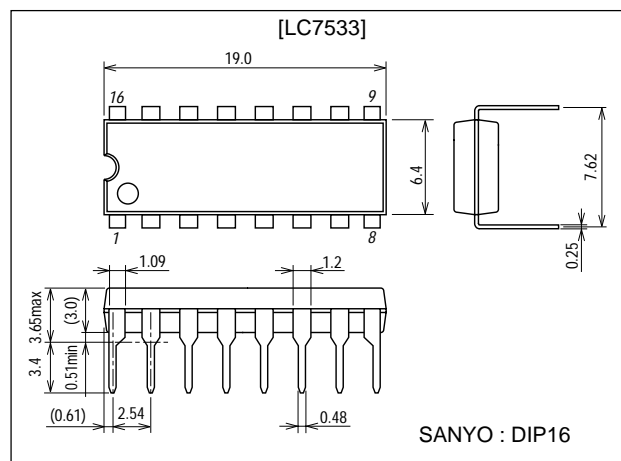
- CMOS process 3V typ. operation.
- Up/down operation is performed with SW input.
- 4-bit, 16-step counter. Step 6\* is set with initial input(INIT).
- Center tap provided.
- Maximum attenuation : -60dB or less.
- Attenuation curve : Pseudo curve A. Left/right simultaneous setting.

\* : Step 6 means mode 6.

### Package Dimensions

(unit:mm)

3006C-DIP16



### Specifications

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}$ max		$V_{SS}$ to 6	V
Supply voltage	$V_I$		$V_{SS}$ to $V_{DD}$	V
Allowable power dissipation	$P_d$ max		100	mW
Operating temperature	$T_{opr}$		-30 to +75	°C
Storage temperature	$T_{stg}$		-40 to +125	°C

#### Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$		2.1 to 5.0	V
Input high-level voltage	$V_{IH1}$	INIT, CE pin	$0.7V_{DD}$ to $V_{DD}$	V
	$V_{IH2}$	UP, DN, CR pin	$0.9V_{DD}$ to $V_{DD}$	V
Input low-level voltage	$V_{IL1}$	INIT, CE	0 to $0.3V_{DD}$	V
	$V_{IL2}$	UP, DN, CR	$V_{SS}$ to $0.1V_{DD}$	V

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# LC7533

## Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Signal distortion	THD <sub>1</sub>	V <sub>DD</sub> =3V, R <sub>L</sub> =50kΩ, f=1kHz			0.5	%
	THD <sub>2</sub>	V <sub>DD</sub> =2.1V, R <sub>L</sub> =50kΩ, f=1kHz		1		%
Output at attenuation mode	X <sub>OUT</sub>	0dBm input, 1kHz, 51kΩ load			-60	dB
Signal transmit delay time	td	Between IN and OUT, no load		1		μs
Input impedance	r <sub>i</sub>	UP, DN, CE only	100		400	kΩ
Output noise voltage	V <sub>NO</sub>	V <sub>DD</sub> =3V, R <sub>L</sub> =50kΩ, STEP" 0"			8	μV
Input high-level current	I <sub>IH</sub>	CE pin, V <sub>DD</sub> =3V, V <sub>I</sub> =3V			40	μA
Input low-level current	I <sub>IL</sub>	UP, DN pin, V <sub>DD</sub> =3V, V <sub>I</sub> =0V	-55			μA
Attenuation balance	ΔV	Pins OUT1, 2, other than STEP" 0" (Note1)	-2	0	+2	dB
Channel balance	ΔV <sub>O</sub>	Between pins OUT1, 2, other than STEP" 0" (Note2)	-2		+2	dB
Current drain	I <sub>DD</sub>	V <sub>DD</sub> =3V, CE=V <sub>DD</sub> , INIT=V <sub>DD</sub> , other pins:OPEN			1	mA
	I <sub>DD</sub> BACK UP	V <sub>DD</sub> =3V, CE=V <sub>SS</sub> , INIT=V <sub>DD</sub> , other pins:OPEN			1	μA
Crosstalk between channels	CT	V <sub>DD</sub> =1.5V, V <sub>SS</sub> =-1.5V, V <sub>M</sub> =0V, f=1kHz, 1Vrms input, test side input : 1kΩ short		85		dB
Minimum pulse width	T <sub>UP/DN</sub>	T=(CR oscillation cycle) UP, DN pin		1.5T		ms
	T <sub>INIT</sub>	INIT pin	2			μs

Note 1 (1)  $\Delta V = 20 \log_{10} V_{OUT} / V_{TYP}$

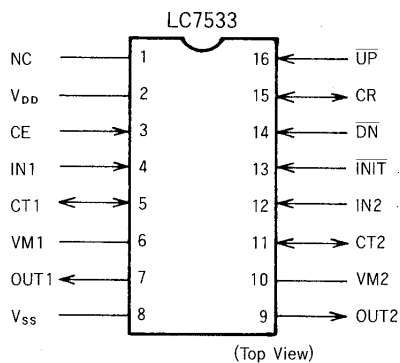
V<sub>OUT</sub> : OUT1(OUT2) output level

V<sub>TYP</sub> : Standard output level

(2) Satisfy V<sub>OUT</sub>(STEP N) < V<sub>OUT</sub>(STEP N + 1)

Note 2 (1)  $\Delta V_O = 20 \log_{10} V_{OUT1} / V_{OUT2}$

## Pin Assignment



Note 1 : No bonding exists on the inside of NC pin.  
It is recommended that the outside should be shorted to V<sub>DD</sub>, V<sub>SS</sub>, etc. on the printed circuit board.

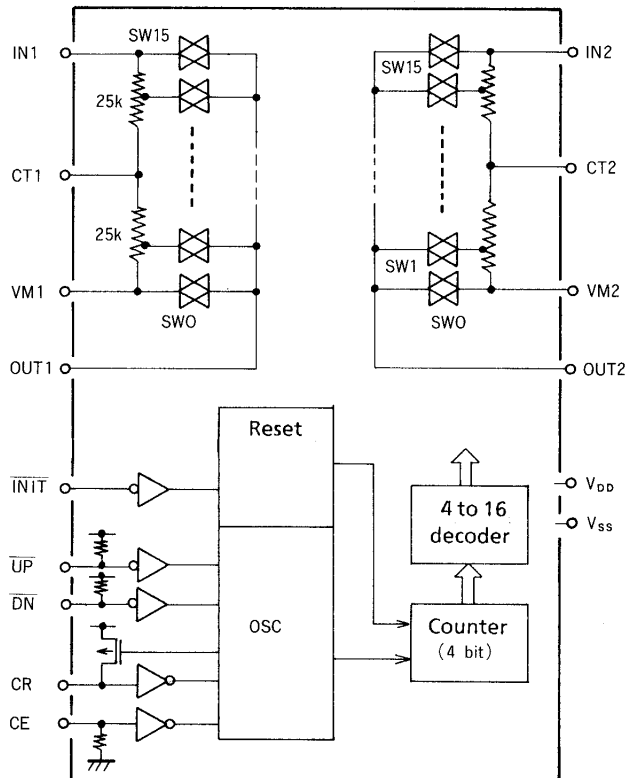
## Pin Description

Pin Name	Pin Number	Description
IN1, IN2	4, 12	Input pin for volume control
OUT1, OUT2	7, 9	Output pin for volume control
V <sub>M1</sub> , V <sub>M2</sub>	6, 10	Bias pin. When operated from single supply, 1/2V <sub>DD</sub> is applied to this pin.
C <sub>T1</sub> , C <sub>T2</sub>	5, 11	Tap pin provided at the center of volume control. By connecting C and R to this pin, the loudness can be controlled.
CE	3	When this pin is set to "L", the current drain is reduced. This pin must be "L" at backup mode.
INIT	13	Initial pin. When set to "L", the 6th step is reached.
UP	16	When the level on this pin is made to fall, the step rises and the volume goes up. When held at "L", the volume goes up; if set to "H", the volume stops going up at a step reached at that moment. The step stops at the MSB position.
DN	14	The DN operation is the reverse of UP. when the UP, DN are set to "L" at the same time, the UP is given priority. The step stops at the LSB position.
CR	15	Pin for connecting R, C on which the rate of step depends.
V <sub>DD</sub>	2	Power supply pin (+)
V <sub>SS</sub>	8	Ground
NC	1	No bonding exists on the inside of NC pin. Connected to V <sub>DD</sub> or V <sub>SS</sub> is recommended.

# LC7533

## Equivalent Circuit Block Diagram

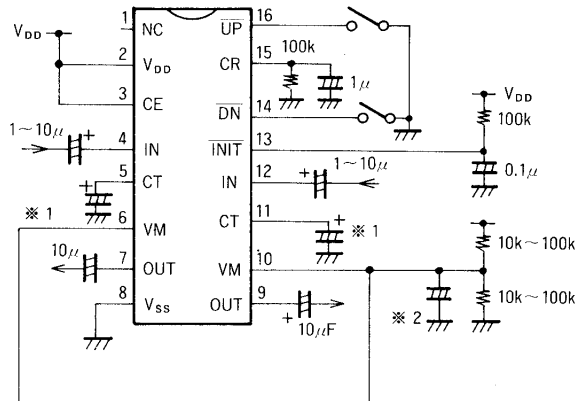
[Common to LC7533]



Note 1 : The TEST pin is bonded only when the MFP20 is used.

## Sample Application Circuit

[LC7533 DIP16]



For  $V_M$ ,  $1/2V_{DD}$  bias is recommended.

※1 For low-band boost (approx.  $1\mu F$ )

※2 The larger the capacity is (approx.  $100\mu F$ ), the better the characteristics of attenuation and crosstalk.

Unit (resistance:  $\Omega$ , capacitance: F)

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